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Abstract
Multiplication operations play an important role in many high-speed DSP and communication systems. For many practical applications, multiplication operations require the fixed-width result so that the n least-significant bits (LSBs) of 2n-bit product must be truncated. The fixed-width property can be applied to significantly reduce the area and power of multiplier by directly omitting about half the adder cells of the conventional multiplier, but an unacceptable product error might be introduced. Many efficient error compensation methods and structures were proposed to reduce the product error. However, most of them designed the fixed-width multiplier based on the Baugh-Wooley multiplier, and none gave attention to the redundant binary signed-digit (RBSD) multiplier. In this thesis, we focus on the design of low-cost truncated RBSD multipliers reduce the area and power of multiplier as well as the whole system. Experimental results show that the proposed fixed-width RBSD multiplier has lower truncation error as compared with other proposed architectures while maintaining smaller area and lower power.

Besides, we use our multiplier to realize a low-cost and high-utilization folded architecture for DCT (discrete cosine transform). The proposed VLSI architecture is described in Verilog HDL and synthesized by the Synopsys Design Compiler with 0.35um 1P4M CMOS technology. The gate count of it is 11040, and chip area is 1745×1734um2. Its operation clock frequency is about 57.8 MHz. Finally, a demo system is built by integrating an Altera FPGA chip implemented the proposed DCT with an 8051 microprocessor to verify the performance of our DCT circuit.
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